

CLAIMS

We claim:

1. A method for producing digital circuitry for use in stackable circuitry
5 comprising the steps of:
coating a surface of a flexible substrate with at least one film;
coating said film on said flexible substrate with a polymer, so as to form at
least one first layered grouping having a top side and a bottom side, said bottom side
being substantially in contact with said flexible substrate;
10 patterning, by lithographical methods, at least one first layered grouping in a
substantially electrically continuous selectively patterned area.
2. A method for producing digital circuitry as claimed in claim 1, wherein
said patterning further comprises patterning said at least one first layered grouping in
15 a substantially electrically continuous selectively patterned area so as to resemble a
substantially waffle shaped pattern.
3. A method for producing digital circuitry as claimed in claim 2,
utilizing an emboss and lift off process, said process further comprising the steps of:
20 effecting said patterning of said substantially waffle shaped pattern by forming
said at least one first layered grouping with a plurality of substantially elongated and
parallel depressions through said top side;
providing a second layered grouping substantially in accordance with said
coating and patterning steps of the first layered grouping;
25 applying said second layered grouping on said top side of said first layered

grouping such that said plurality of substantially elongated and parallel depressions of the second layered grouping are in a substantially orthogonal juxtaposition with said plurality of substantially elongated and parallel depressions of the first layered grouping

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4. A method for producing digital circuitry as claimed in claim 3, utilizing an emboss and lift off process, said process further comprising the steps of:
- coating a surface of a flexible substrate with at least one film;
 - coating said film on said flexible substrate with a polymer, so as to form a first
 - 10 layered grouping having a top side and a bottom side, said bottom side being substantially in contact with said flexible substrate;
 - embossing a plurality of depressions having trench portions on said polymer;
 - patterning said first layered grouping by etching of an area comprising said
 - plurality of depressions through to said surface of said substrate substantially
 - 15 contiguous with the trench portions of said depressions within said first layered grouping;
 - applying an adhesive layer to said top side of said first layered grouping;
 - peeling off said substrate from said bottom side of said first layered grouping
 - so as to reveal a substantially planar surface on said bottom side;
 - 20 providing a second layered grouping substantially in accordance with said coating, forming, embossing and patterning steps of the first layered grouping;
 - applying said second layered grouping on said top side of said first layered grouping in a substantially orthogonal juxtaposition.

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5. A digital circuitry system comprising:

a memory module having a plurality of stackable cross-point memory arrays stacked so as to have interconnection in a unitary package; and

a plurality of conductive pads, said conductive pads adapted for providing said
5 interconnection of said stacked cross-point memory arrays through a patterned waffle structure.

6. The digital circuitry system as claimed in claim 5, wherein said

patterned waffle structure of said conductive pads is formed from at least two
10 separately patterned groupings of layered materials which are combined together, in substantially the same planar direction, at a substantially orthogonal juxtaposition.

7. The digital circuitry system as claimed in claim 6, wherein said

at least two separately patterned groupings of layered materials are formed from the
15 application of at least one thin film on a flexible substrate.